Principle of EE1
Lesson 4

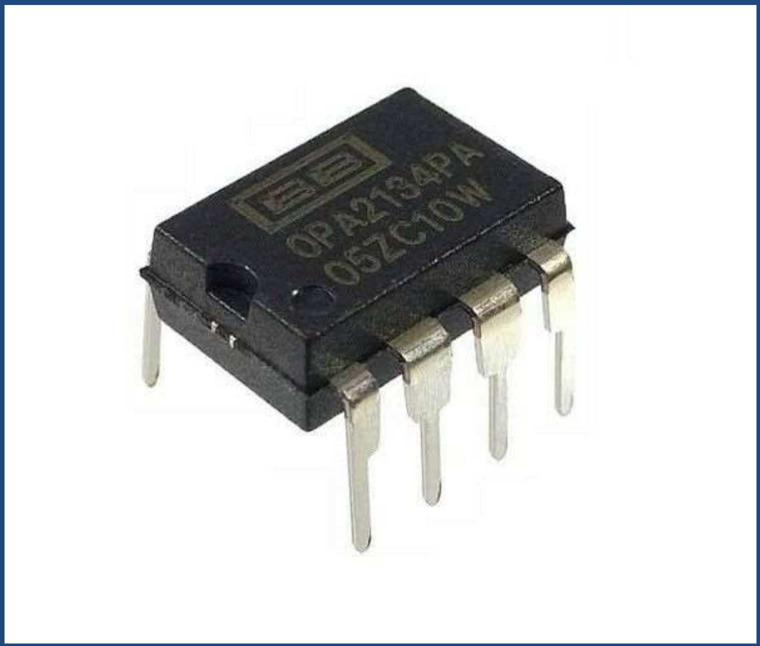
Prof. Võ Văn Tới
School of Biomedical Engineering
Vice-Provost for Life and Health Science, Engineering and Technology Development of International University
Vietnam National Universities – HCMC

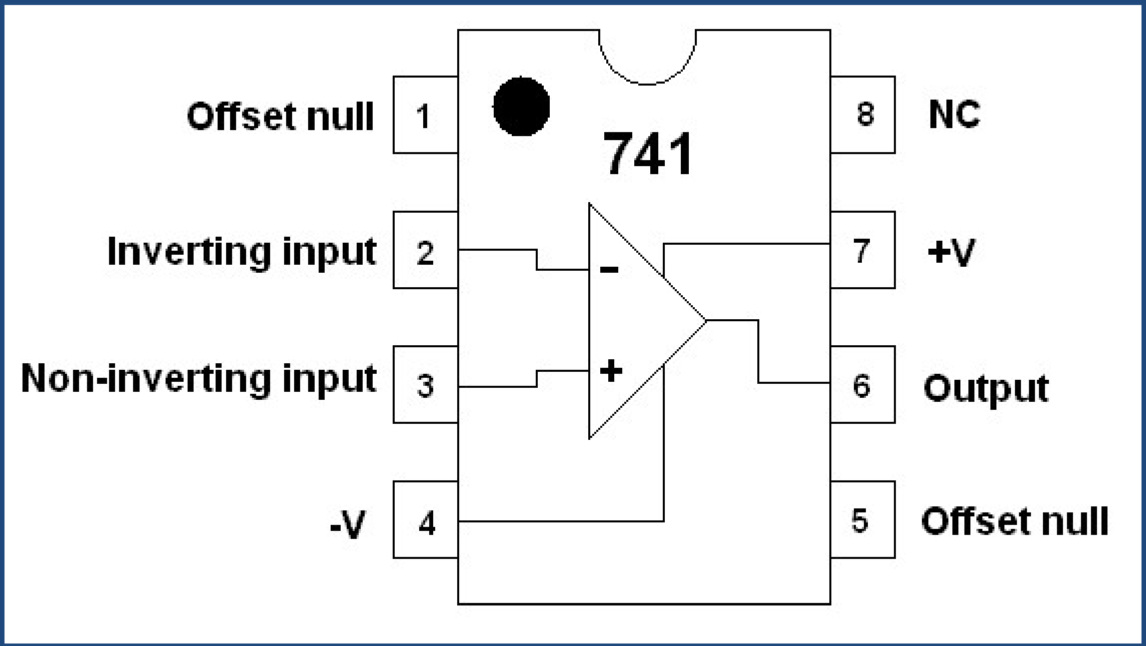
OPERATIONAL AMPLIFIER (OP-AMP)

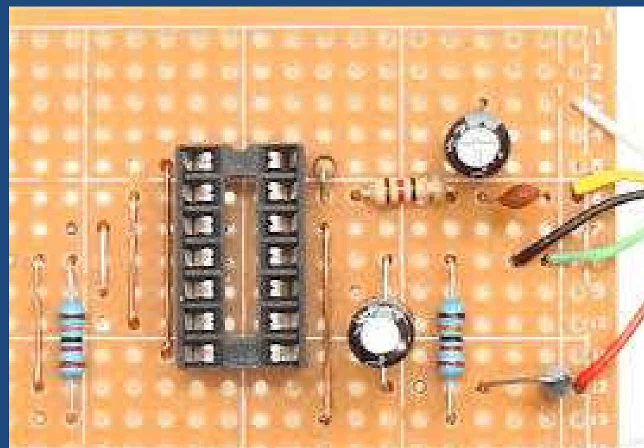
Contents

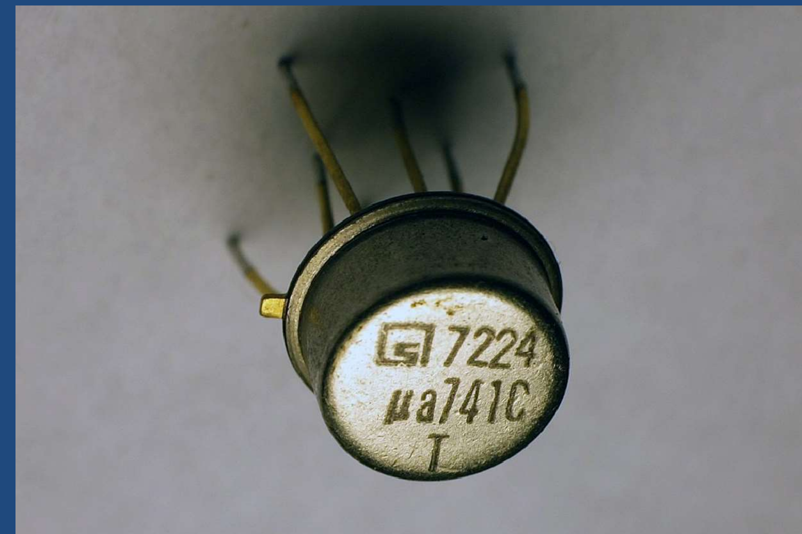
- Physical aspect of an op-amp
- Op-amp characteristics
- Negative feedback circuit:
  - Applications of op-amp
  - Analysis of an op-amp circuit
  - Different features of op-amp utilization
- Real world op-amp

OPERATIONAL AMPLIFIER (Op-Amp)





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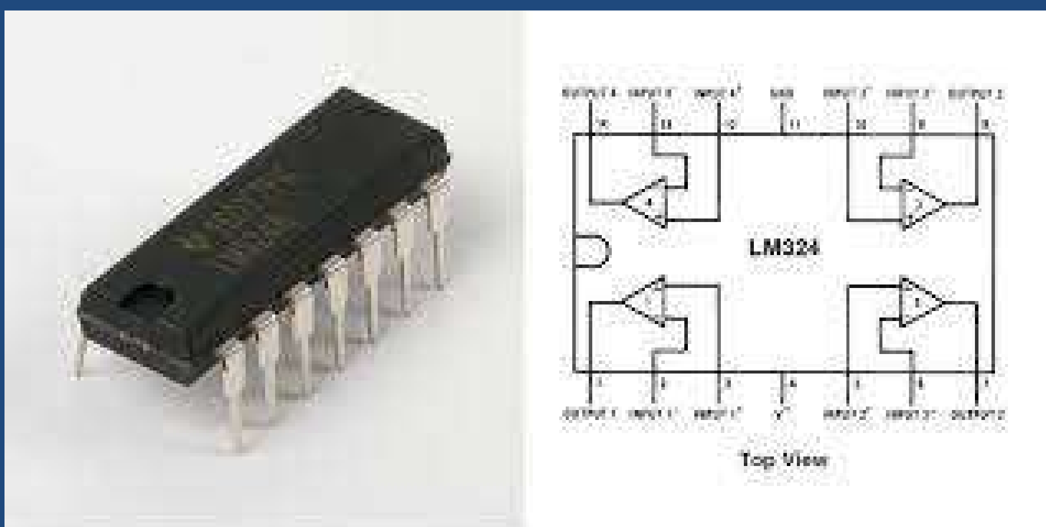
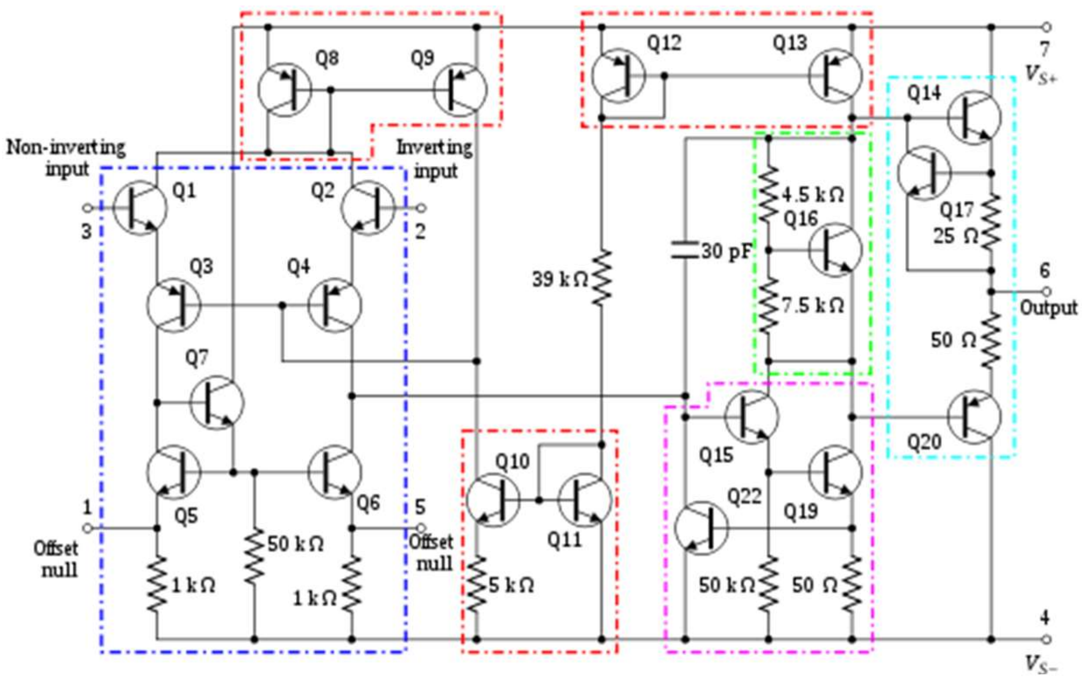
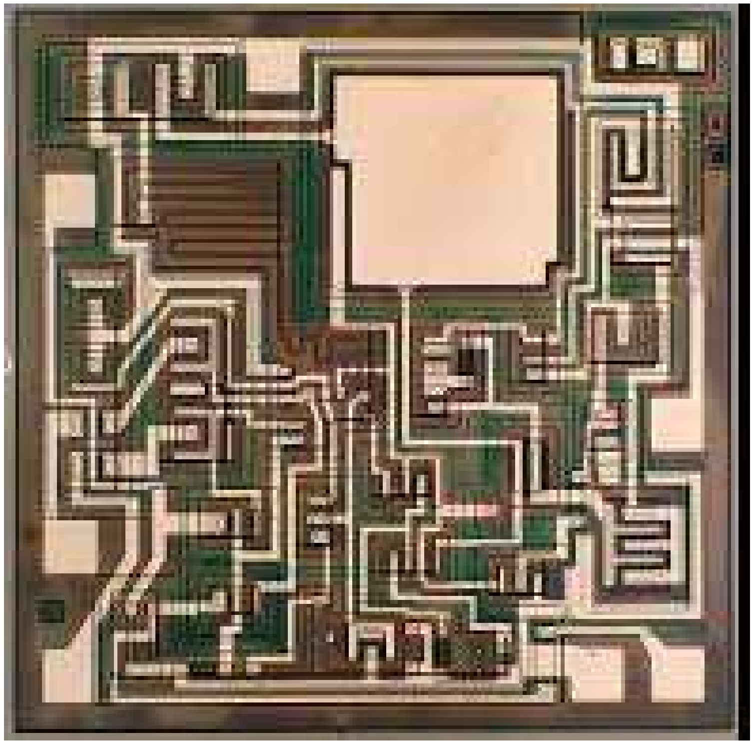
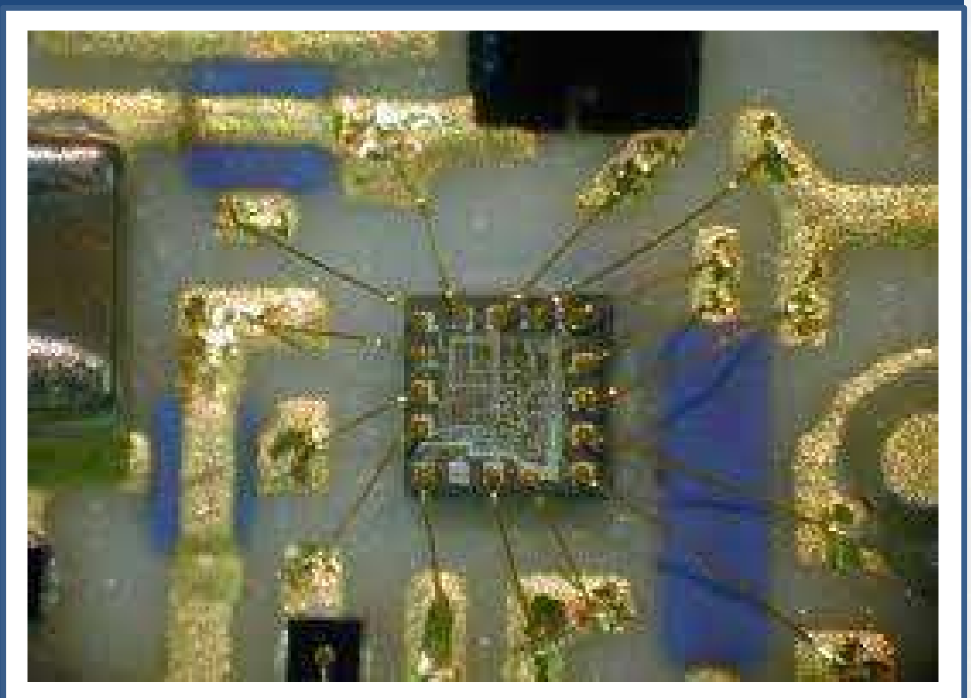

LM324
Top View

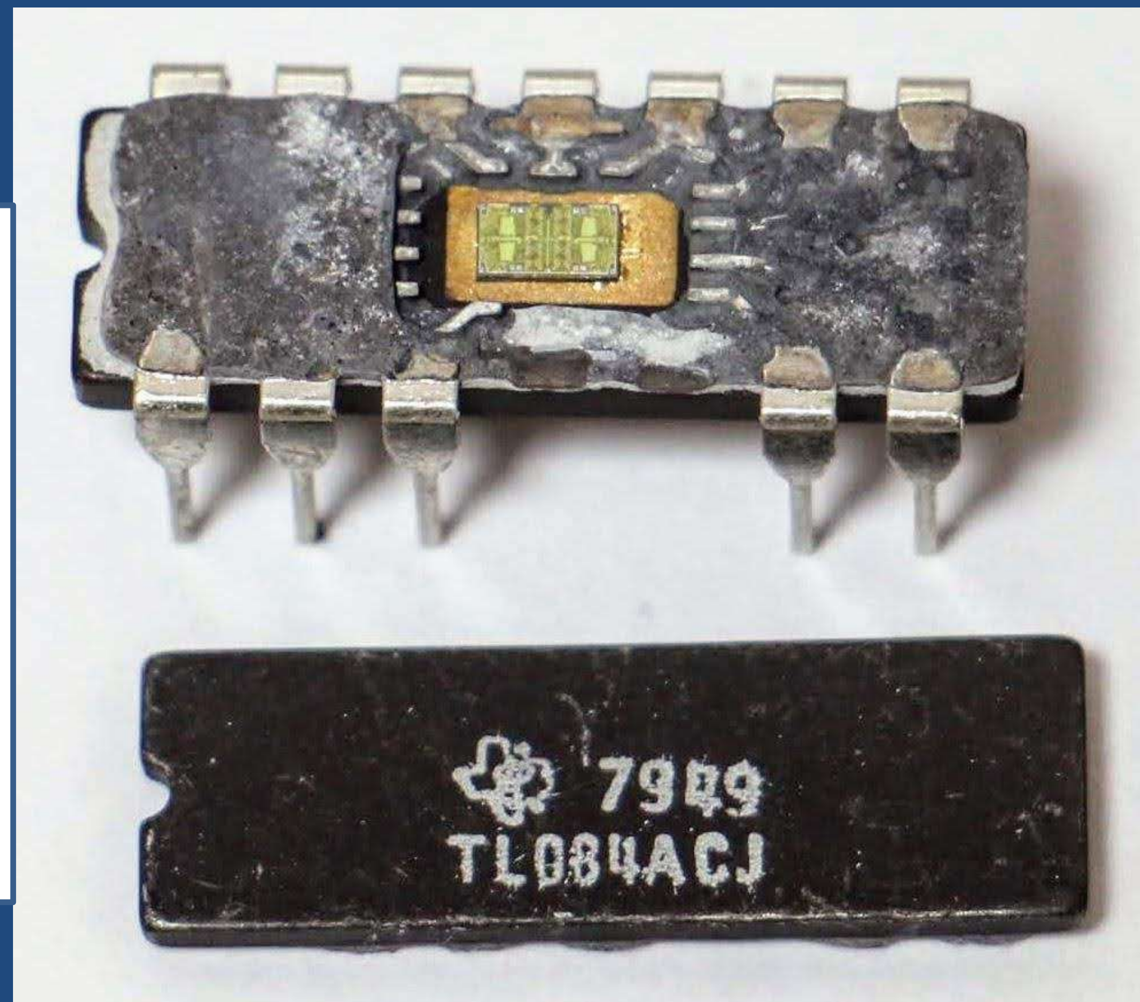

MPA4609
TEXAS INSTRUMENTS

Very large-scale integration (VLSI) Technology





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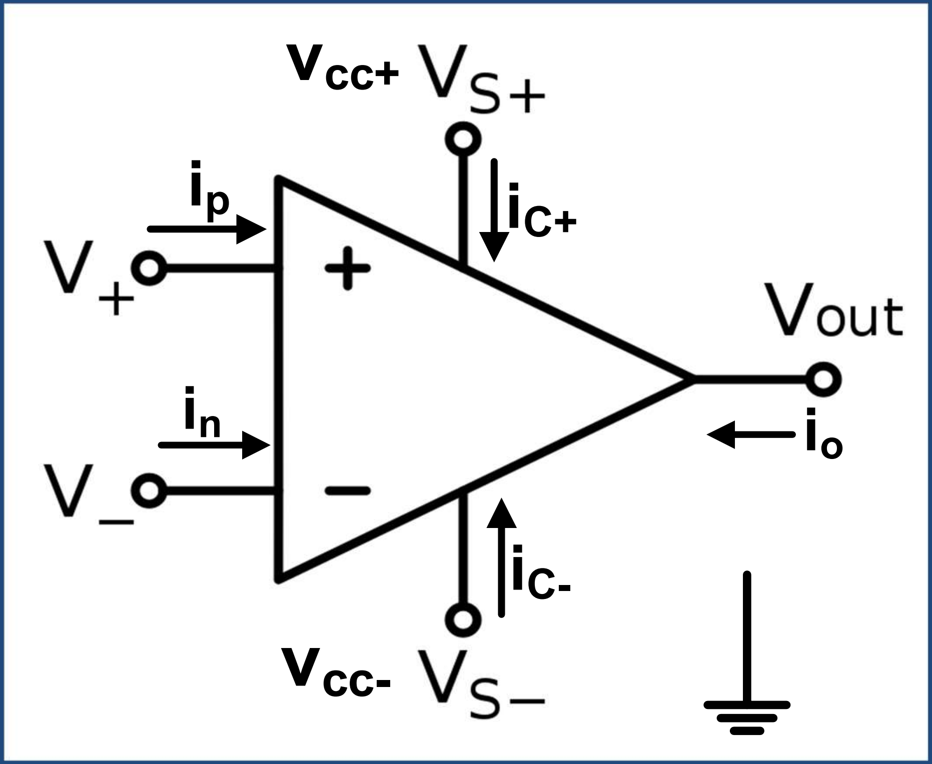
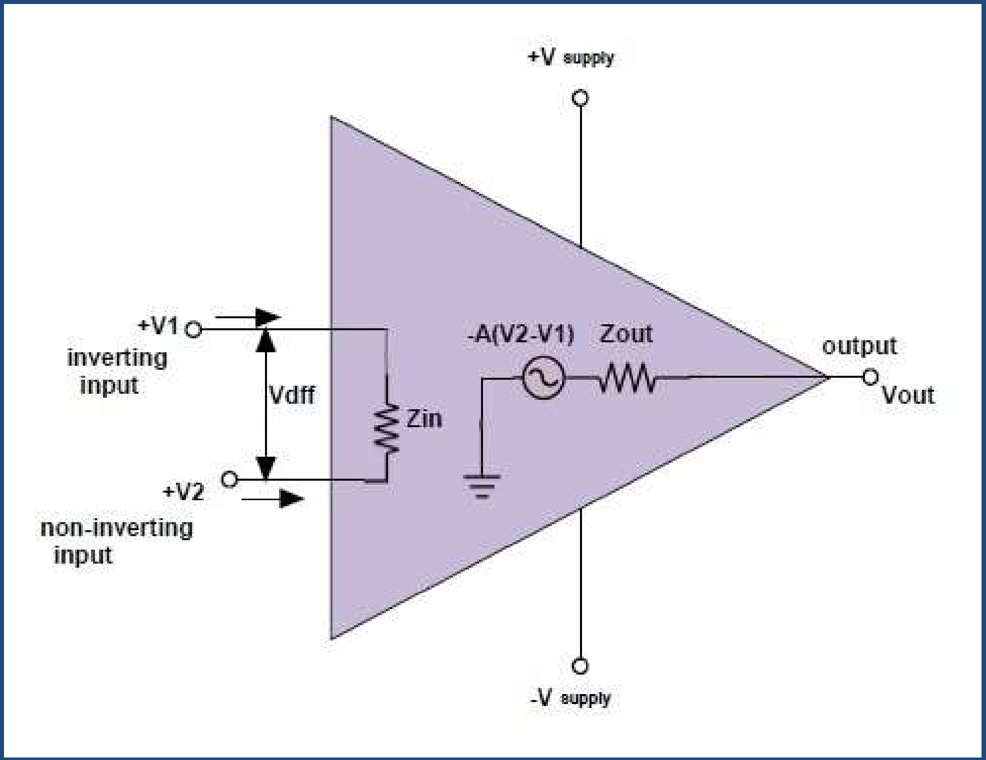
Op-Amp Basics



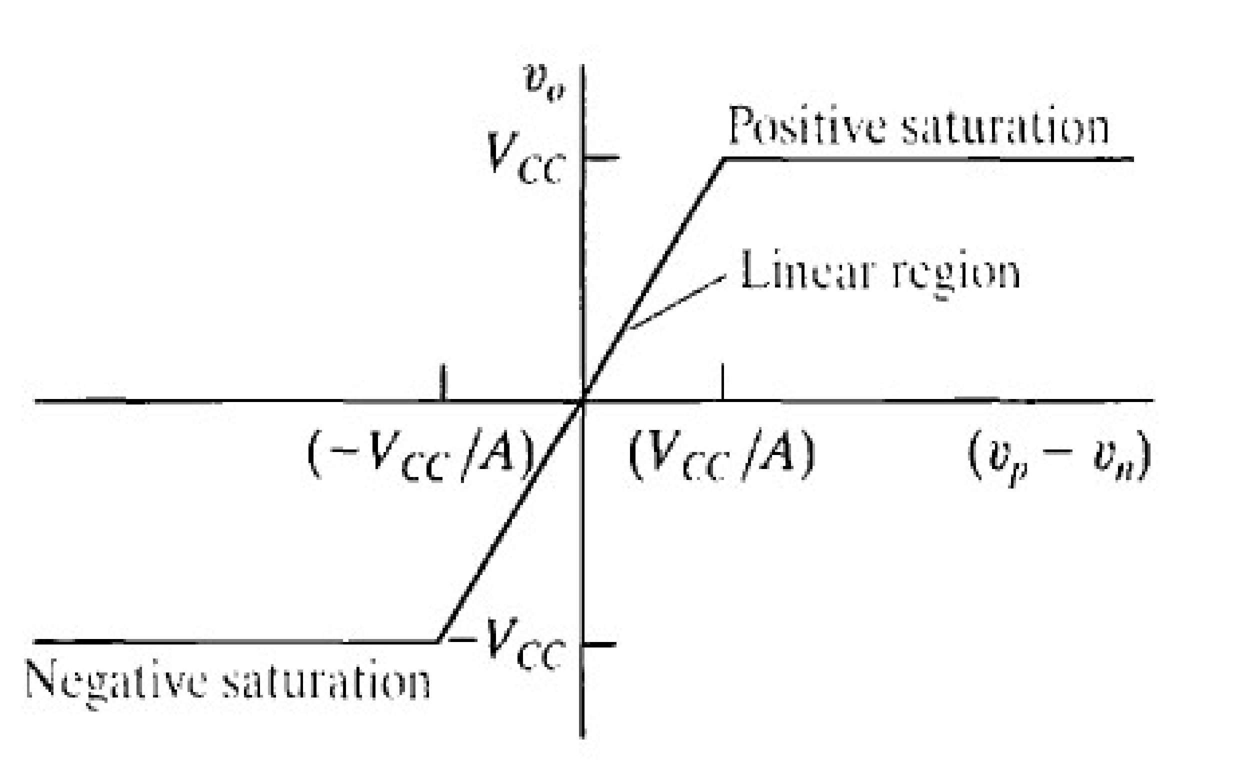
Ideal op-amp



Real op-amp

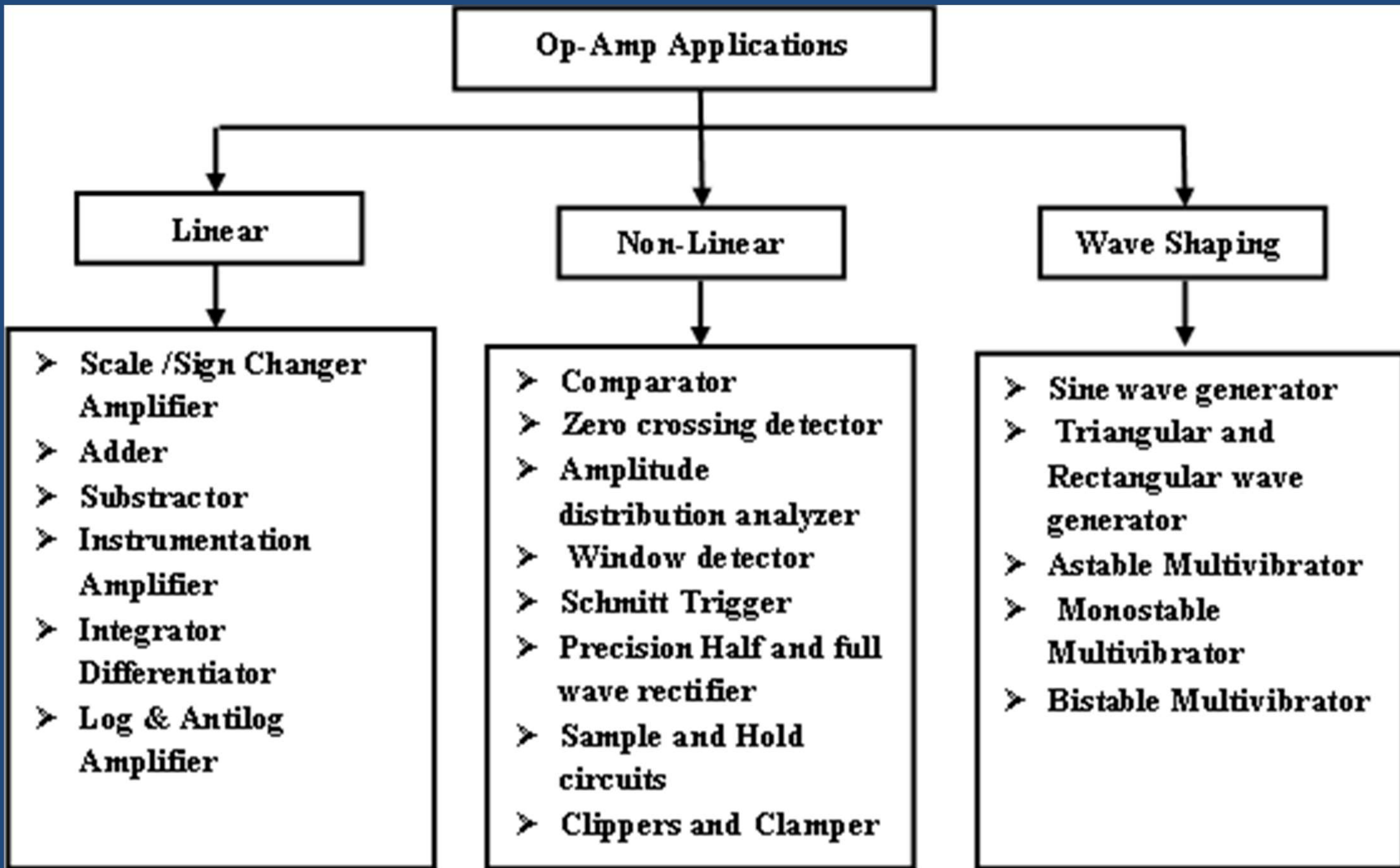
Characteristics of an ideal op-amp

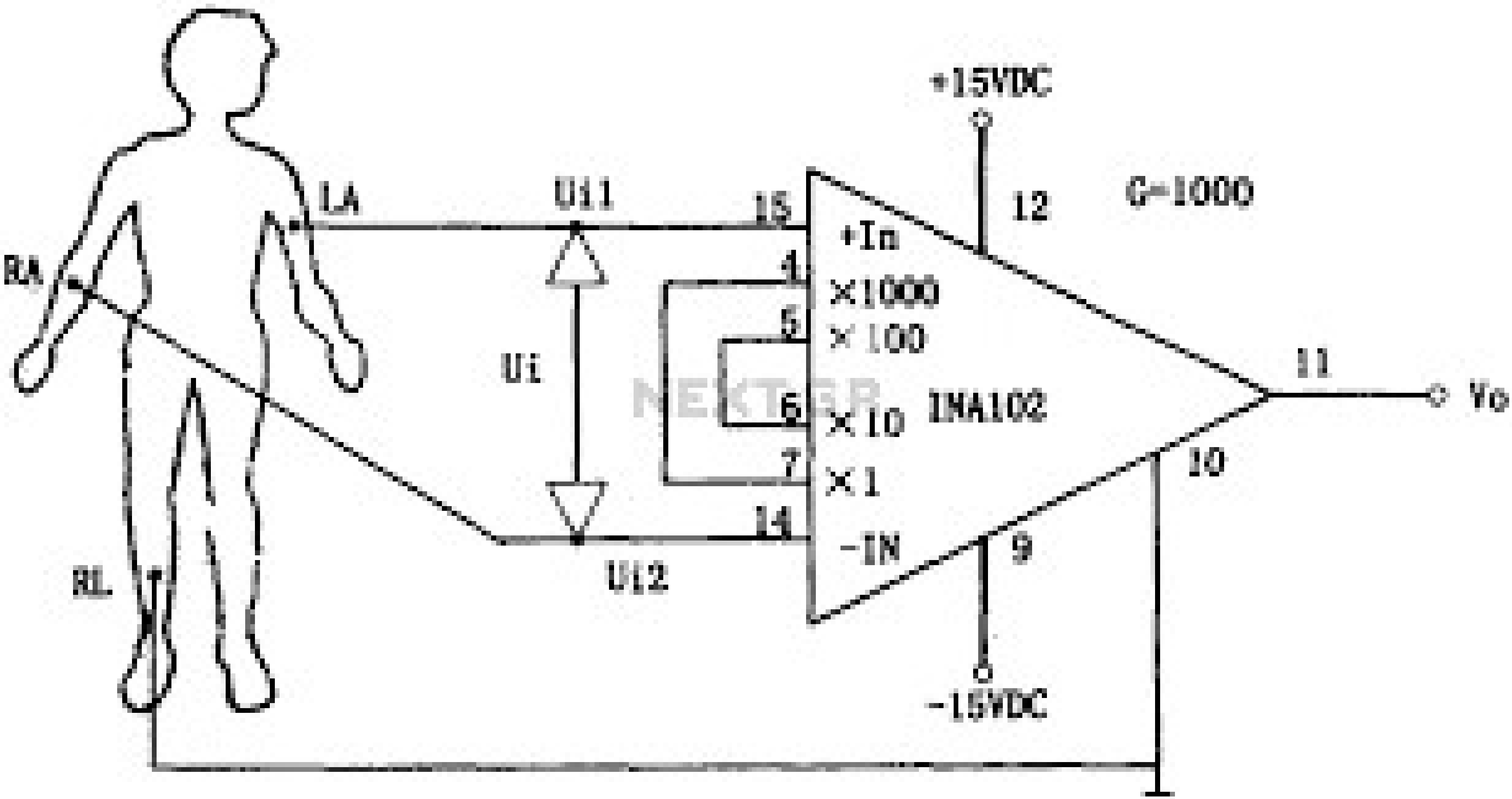
1. Linear vs. saturated zones



Characteristics of an ideal op-amp

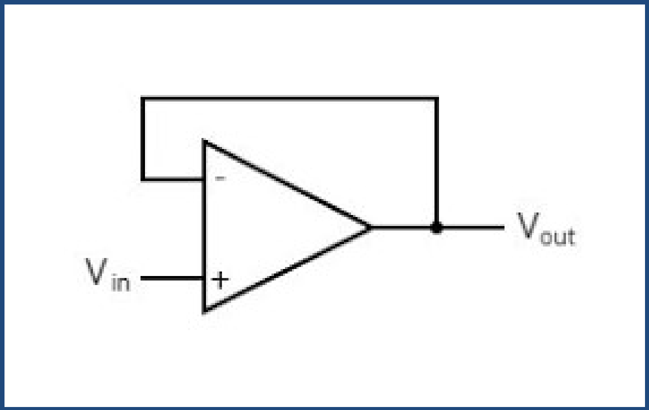
1. Linear vs. saturated zones
2. Infinite input impedance => $I_p = I_n = 0$
3. Zero output impedance
4. Infinite voltage gain
5. Zero common mode gain
6. Infinite bandwidth

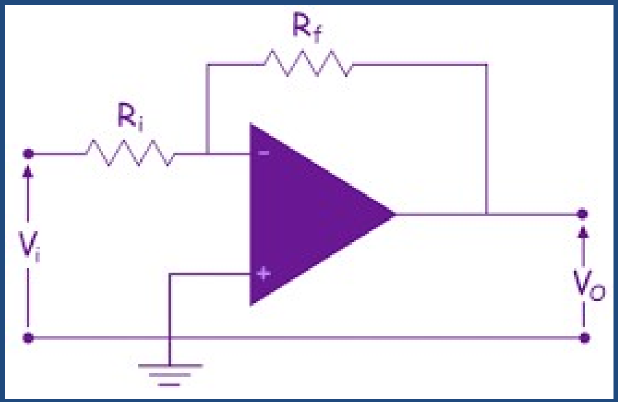

Op-Amp Applications
Linear
Non-Linear
Wave Shaping
Scale /Sign Changer Amplifier
Adder
Substractor
Instrumentation Amplifier
Integrator Differentiator
Log & Antilog Amplifier
Comparator
Zero crossing detector
Amplitude distribution analyzer
Window detector
Schmitt Trigger
Precision Half and full wave rectifier
Sample and Hold circuits
Clippers and Clamper
Sine wave generator
Triangular and Rectangular wave generator
Astable Multivibrator
Monostable Multivibrator
Bistable Multivibrator

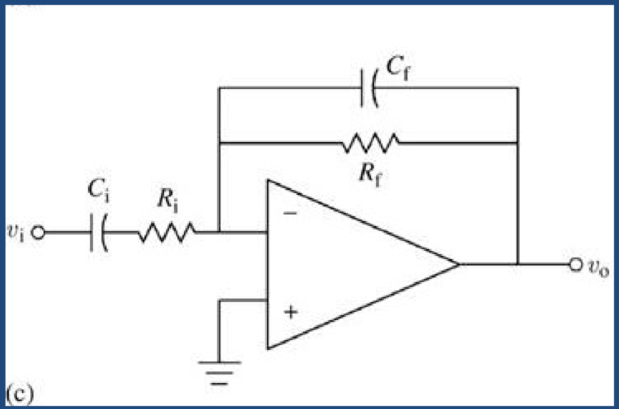

+15VDC
G=1000
LA
U11
15
12
+In
RA
4
×1000
5
× 100
Ui
6
× 10
INA102
11
Vo
7
× 1
10
14
-IN
9
RL
U12
-15VDC

Negative Feedback

1. $v_p = v_n$
2. $i_p = i_n = 0$



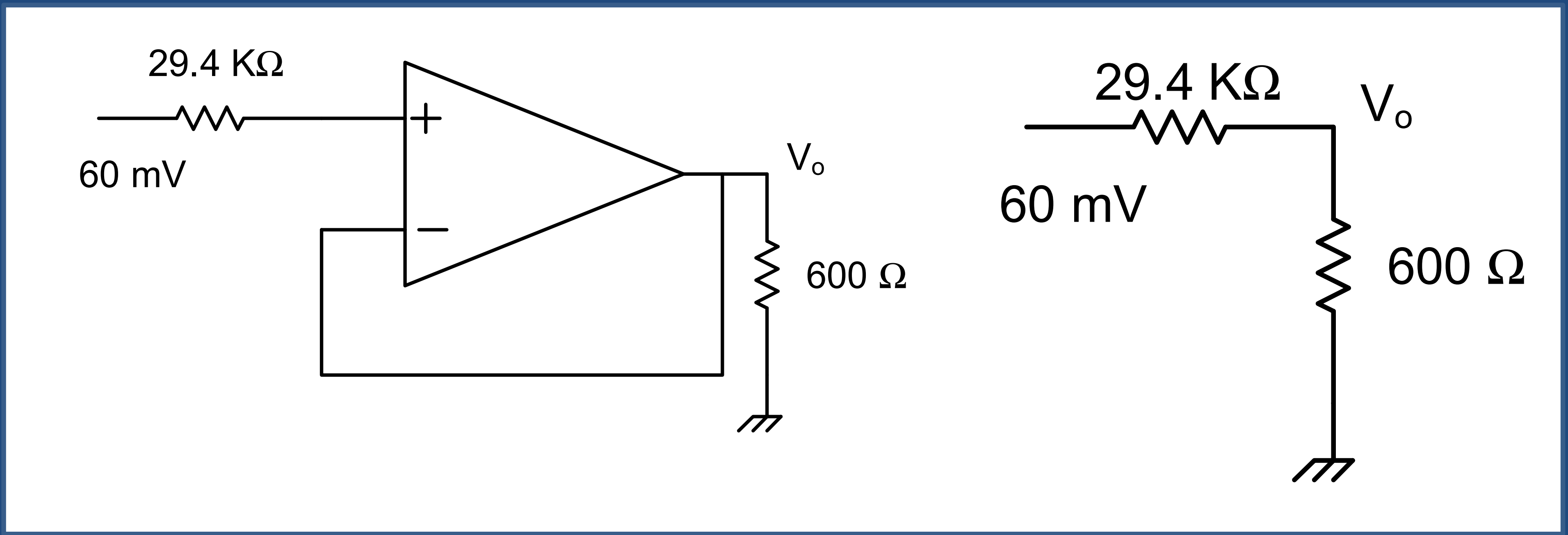




ANALYSIS OF A CIRCUIT USING OP-AMP

Role of an Op-Amp

What are the gains in voltage and power at 600Ω in both situations?



Role of an Op-Amp (cont.)

* With op-amp:

$i_p = i_n = 0$

$v_p = v_n = 60x10^{-3}V$

$v_o = v_{in} = 60x10^{-3}$ (voltage follower)

$P = (0.06)^2/600 = 6x10^{-6}$ W

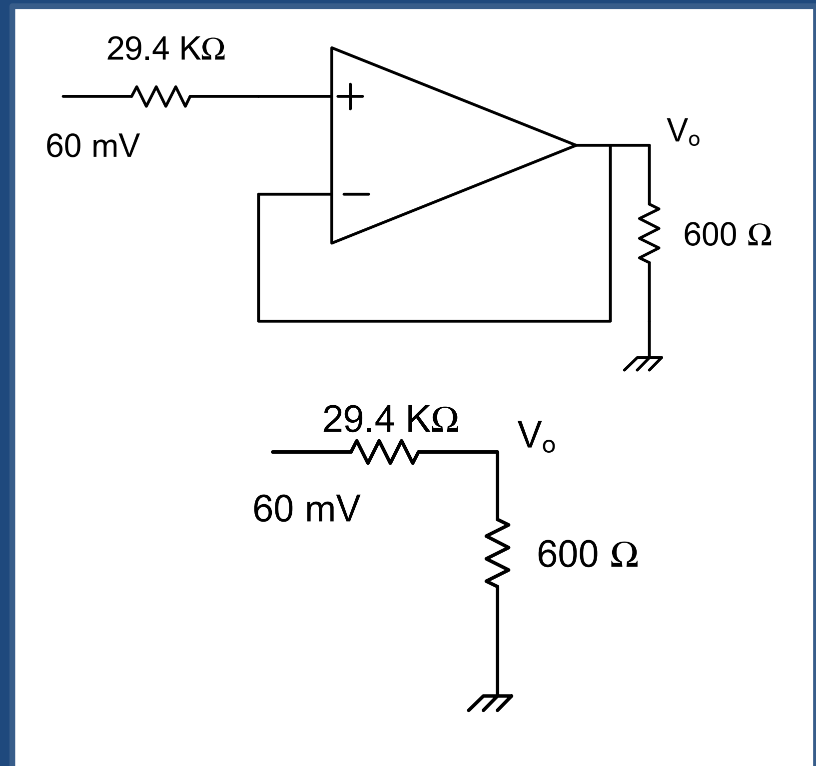
* Without op-amp:

$$v_0 = 60.10^{-3} \frac{600}{29{,}400+600} = 1.2x10^{-3}V$$

$P = (1.2x10^{-3})^2 /600 = 2.4x10^{-9}W$

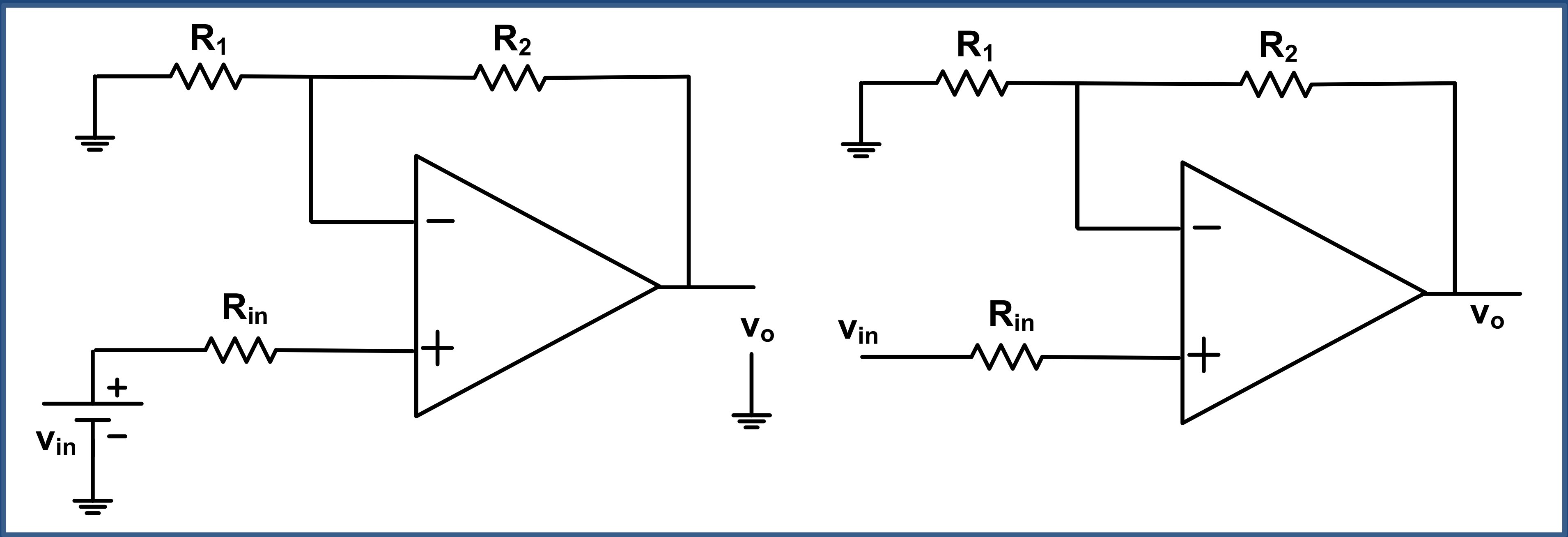
With op-amp: Voltage gain 50X and

Power gain 2.500X



Non-Inverting input

Given v_{in} and all resistances. Find relationship between v_o and v_{in}



Non-Inverting input (cont.)

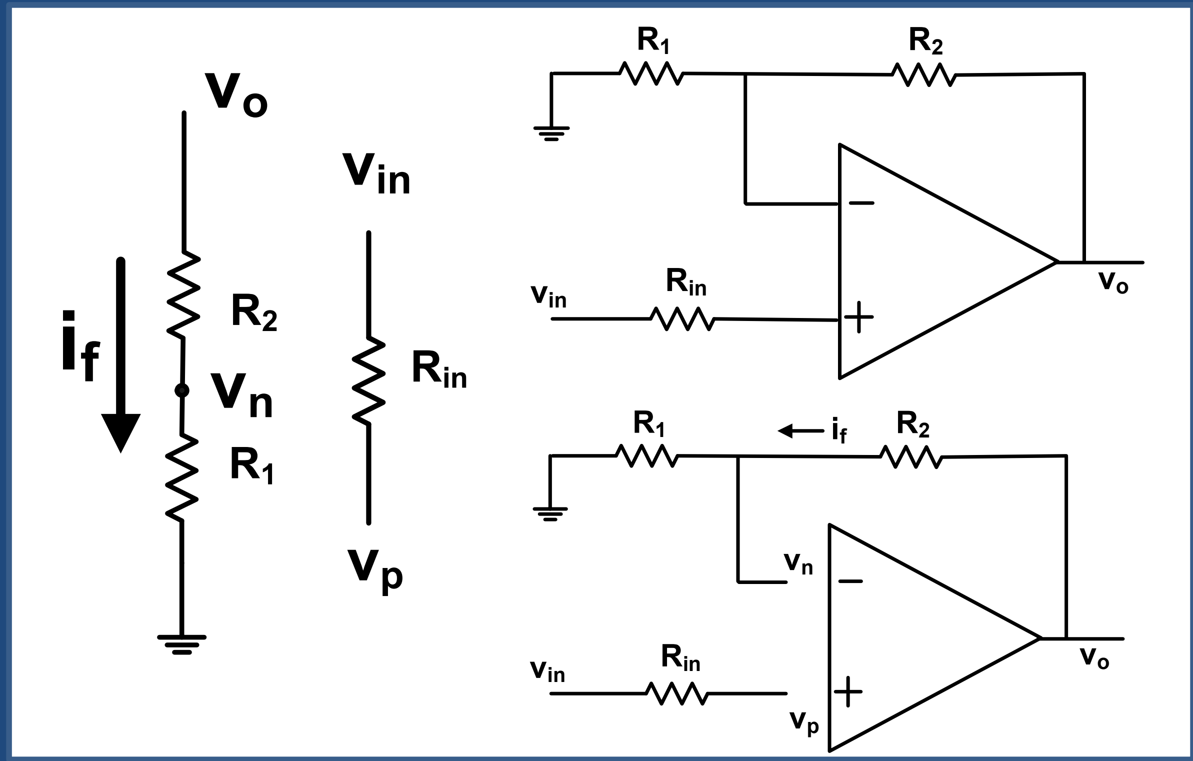
1. $i_p = i_n = 0$
2. $v_p = v_n$

$V_p = v_{in}$

Using voltage divider

$$v_n = v_o \frac{R_1}{R_1 + R_2} = v_{in}$$

$$\Rightarrow \mathbf{v_o = v_{in} \frac{R_1 + R_2}{R_1}}$$

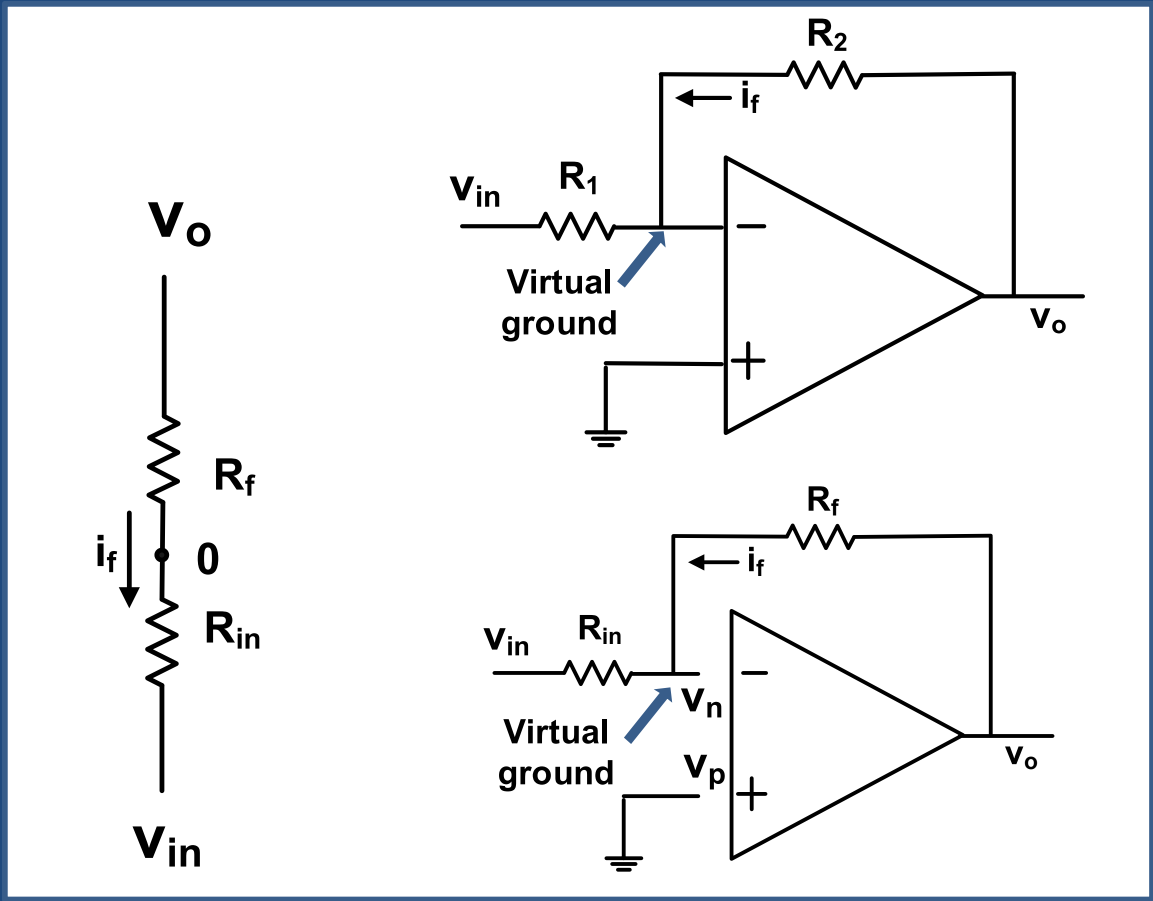


Inverting input

1. $i_p = i_n = 0$
2. $v_p = v_n = 0$

$$i_f = \frac{v_o}{R_f} = \frac{0 - vin}{R_{in}}$$

$$\Rightarrow \mathbf{v_o = -v_{in}\frac{R_f}{R_{in}}}$$



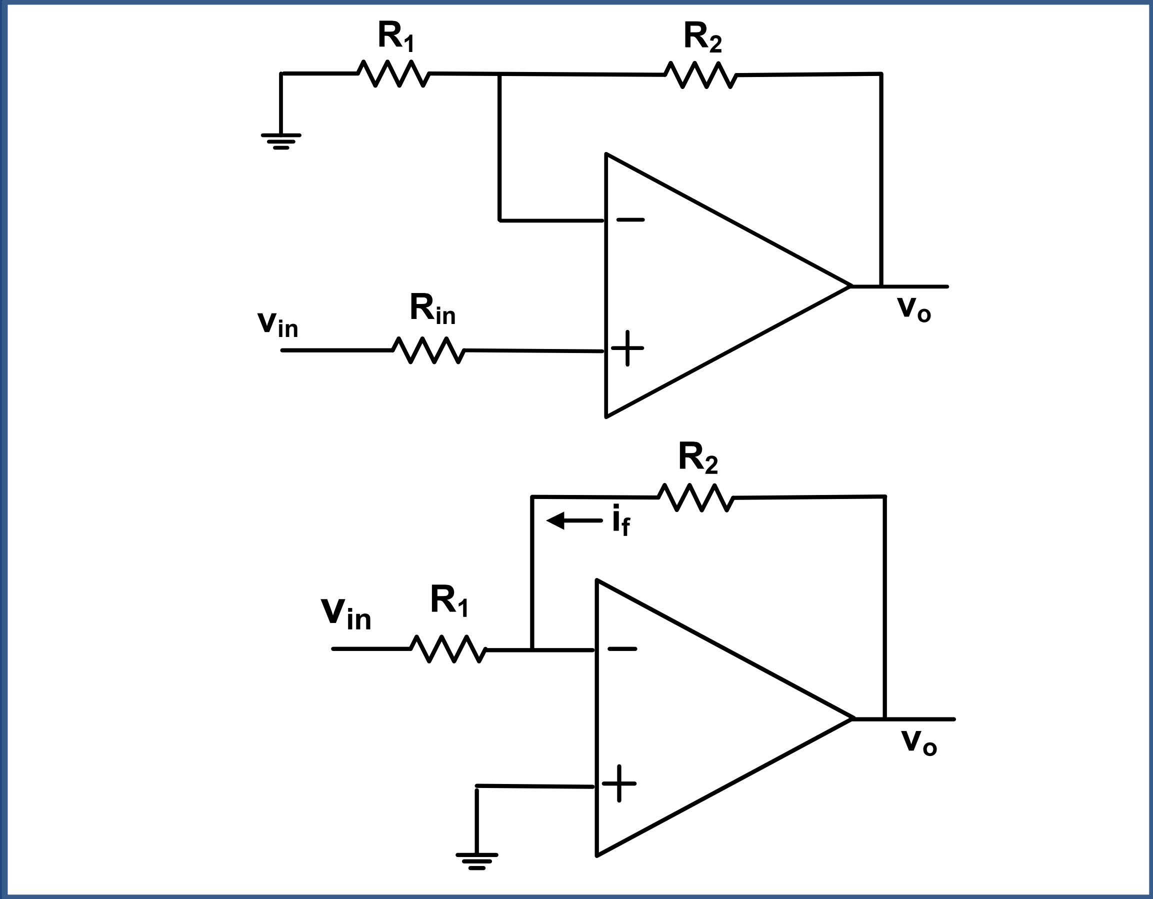
Comparison between Non-Inverting and Inverting input features

$$v_o = v_{in}\frac{R_1 + R_2}{R_1}$$

$v_o \geq v_{in}$ and same sign

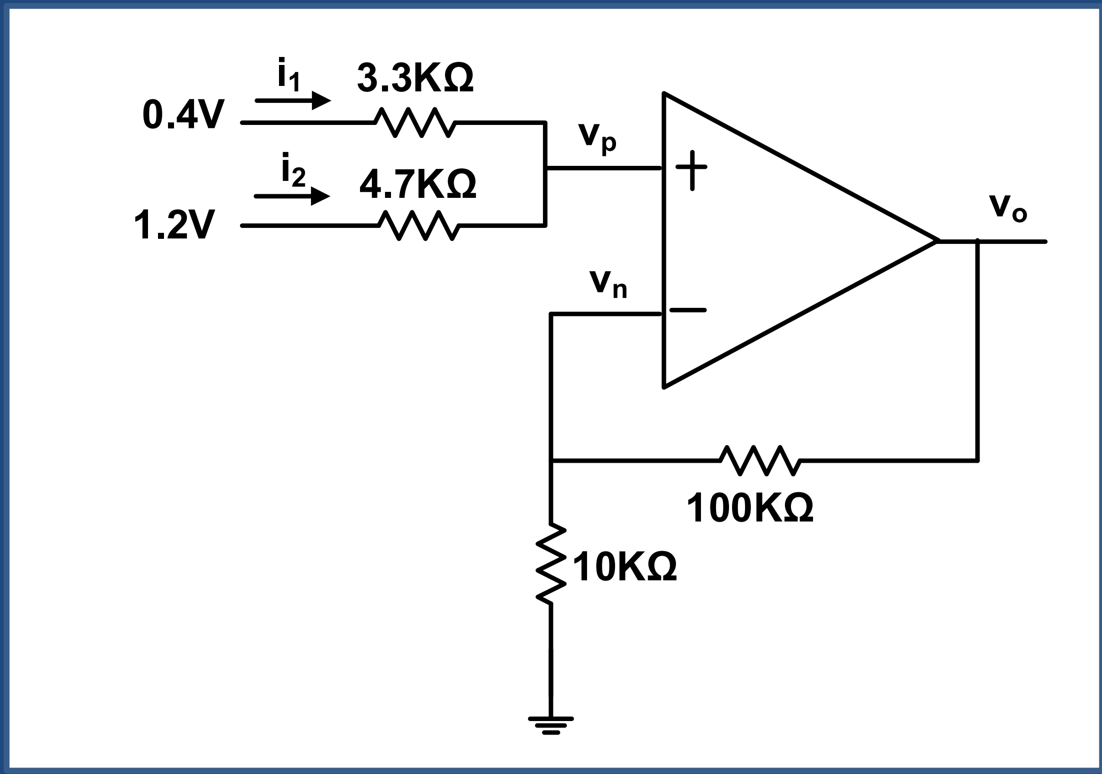
$$v_o = -v_{in}\frac{R_2}{R_1}$$

$v_o \geq v_{in}$ or $v_o \leq v_{in}$ and in opposite sign



Adding 2 non-inverting inputs

Determine v_p and v_o



Solution

1. $i_p = i_n = 0$
2. $v_p = v_n$

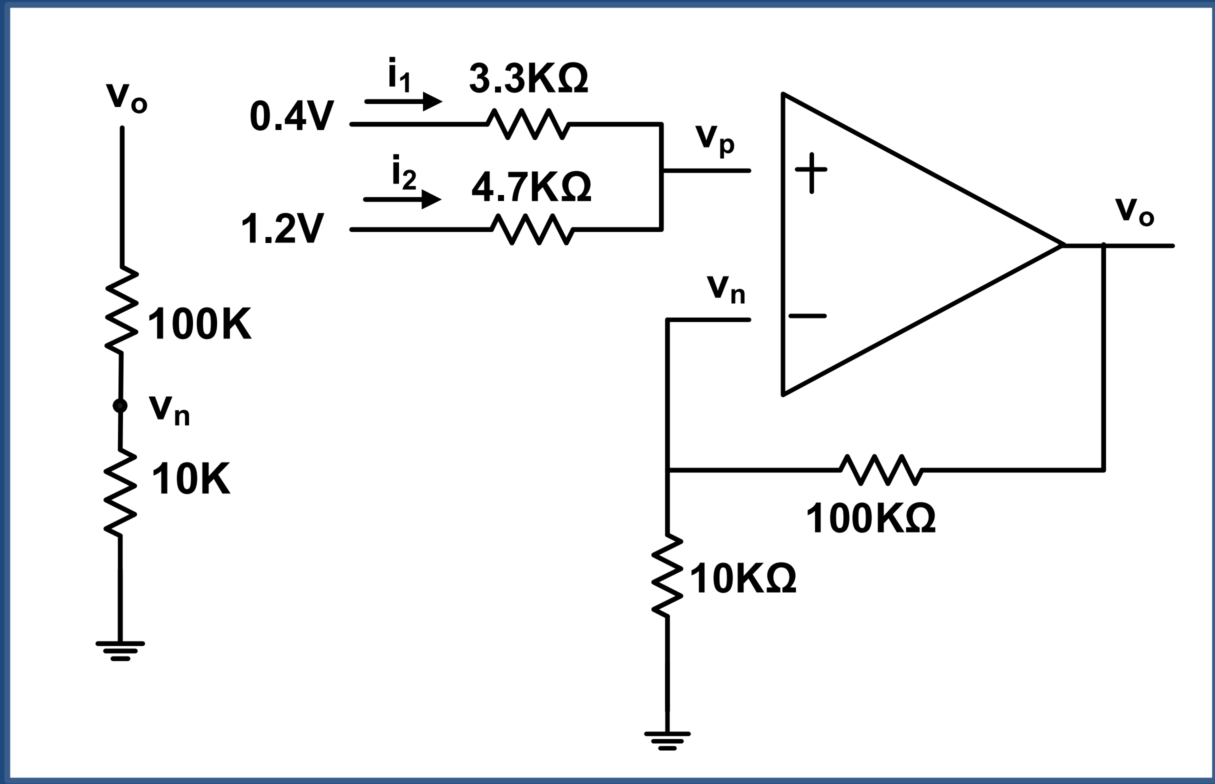
$i_1 + i_2 = 0$

$$\frac{0.4 - vp}{3.3K} + \frac{1.2 - vp}{4.7K} = 0$$

$$\Rightarrow v_p = \underline{\mathbf{0.73V}}$$

$$v_n = v_o \frac{10K}{10K + 100K} = v_p$$

$$\Rightarrow v_o = 11\, v_p = \underline{\mathbf{8.03V}}$$

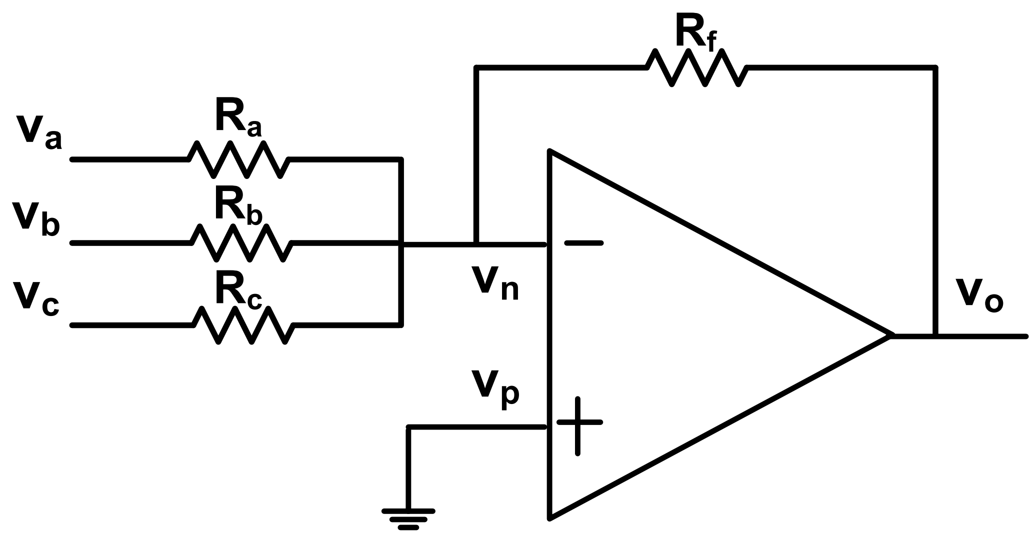


Adding 3 inverting inputs: Summer

1. $i_p = i_n = 0$
2. $v_p = v_n = 0$

$$\frac{v_a}{R_a} + \frac{v_b}{R_b} + \frac{v_c}{R_c} = -\frac{v_o}{R_f}$$

$$\Rightarrow v_o = -R_f\left(\frac{v_a}{R_a} + \frac{v_b}{R_b} + \frac{v_c}{R_c}\right)$$



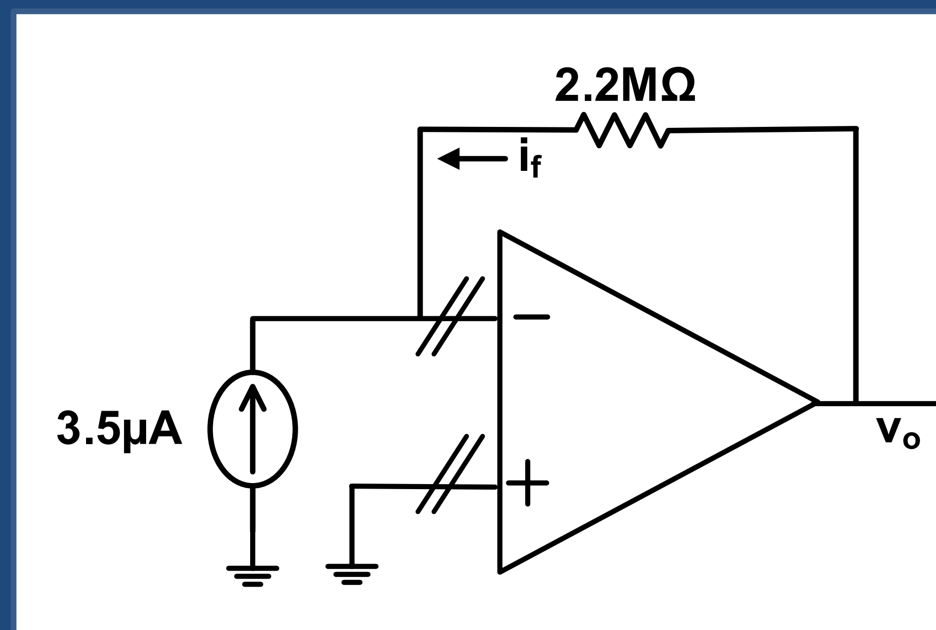
Current to Voltage Converter

The goal of this circuit is to convert a current source into a voltage source

1. $i_p = i_n = 0$
2. $v_p = v_n = 0$

$i_f = -3.5\ \mu A$

$\Rightarrow v_o = 2.2.10^6\,(-3.5\text{x}10^{-6}) = \mathbf{-7.7\ V}$



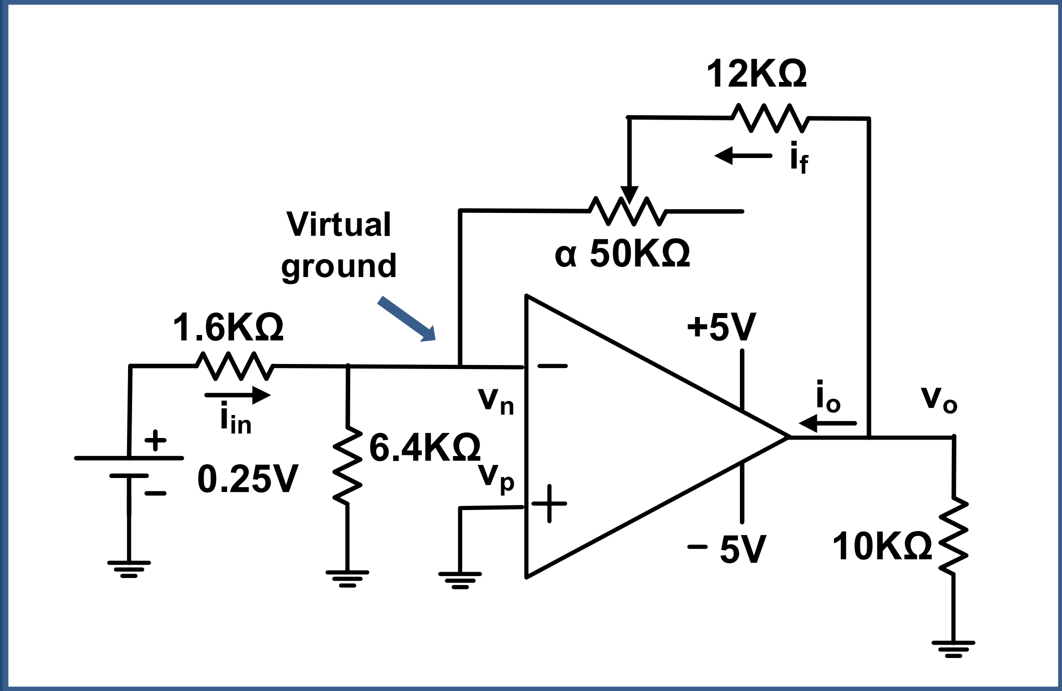
Example

Find the range of α so that the op-amp is not saturated

$\Rightarrow V_o \leq +5V$
Or $V_o \geq -5V$
And $0 \leq \alpha \leq 1$

Statement:

1. $i_p = i_n = 0$
2. $v_p = v_n = 0$



Solution

$$i_{in} = \frac{0.25}{1.6K} = -\, i_f$$

$$v_o = \mathbf{i_f}\,(\alpha\ 50K + 12K)$$

$$v_o = -\,\frac{0.25}{1.6K}(\alpha\ 50K + 12K)$$

$$= -\,0.16\,(\alpha\ 50 + 12)$$

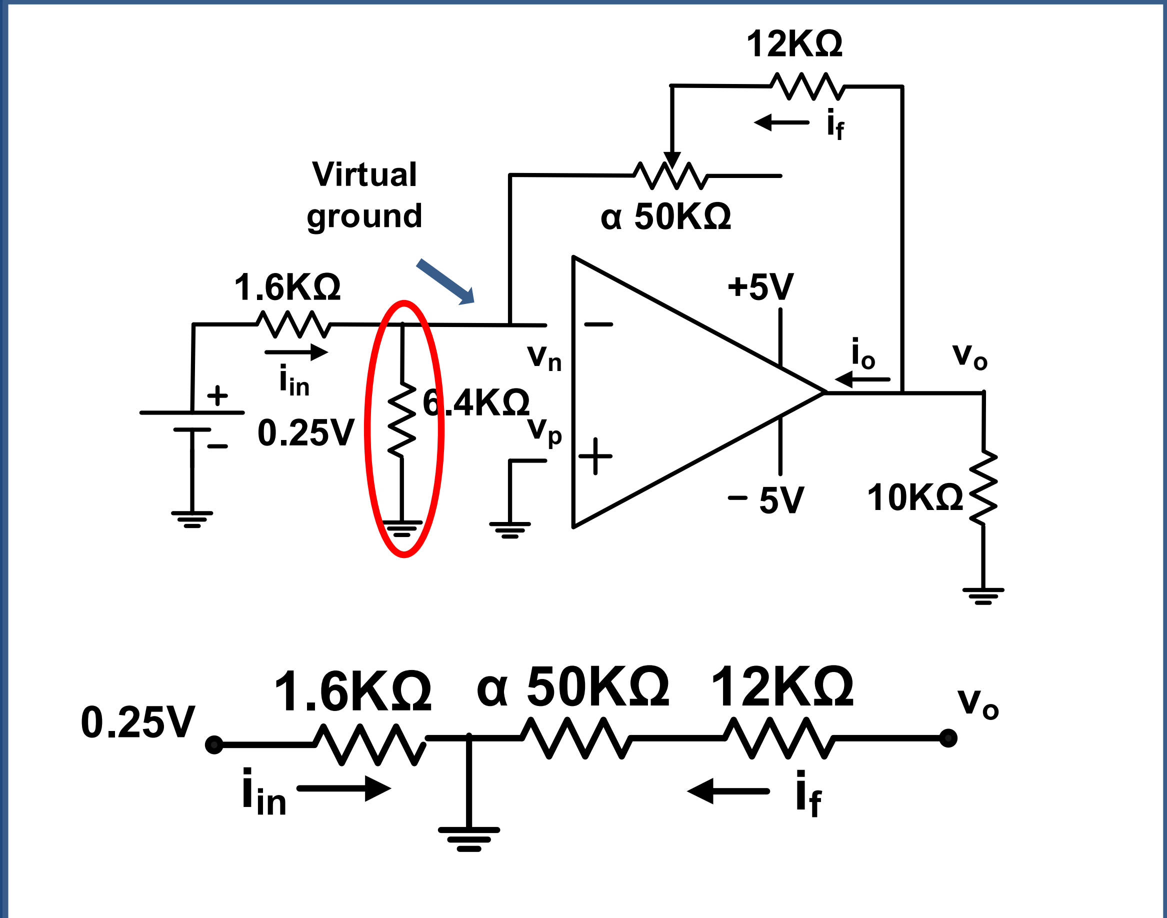
* $\underline{V_o \geq -\,5V}$

=> $\alpha \leq 0.4$

* $\underline{V_o \leq +\,5V}$

=> $\alpha \geq -\,0.88$

Therefore **$0 \leq \alpha \leq 0.4$**

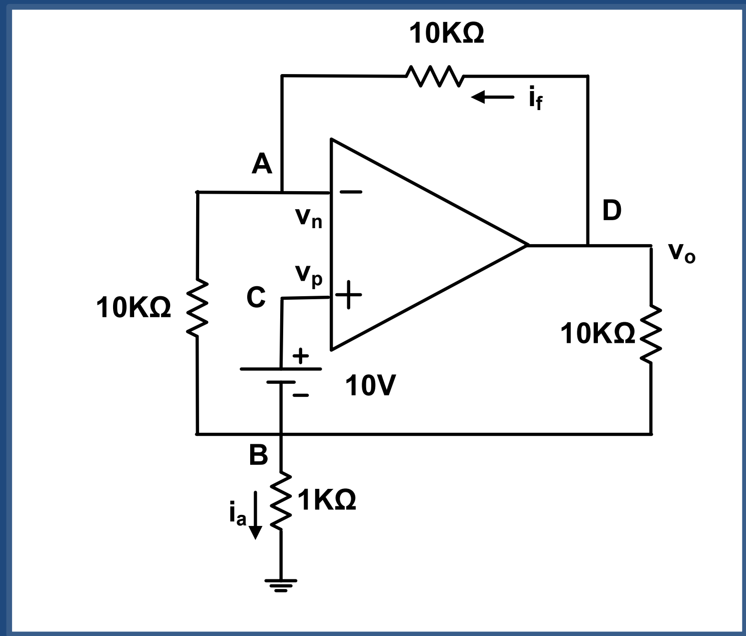


Exercise

Find the current i_a

Statement:

1. $i_p = i_n = 0$
2. $v_p = v_n$



Solution

Use node technique:

A: $\left(\frac{1}{10K}+\frac{1}{10K}\right)v_A - \frac{1}{10K}v_B - \frac{1}{10K}v_o = 0$ (1)

B&C: $-\frac{1}{10K}v_A + \left(\frac{1}{1K}+\frac{1}{10K}+\frac{1}{10K}\right)v_B - \frac{1}{10K}v_o = 0$ (2)

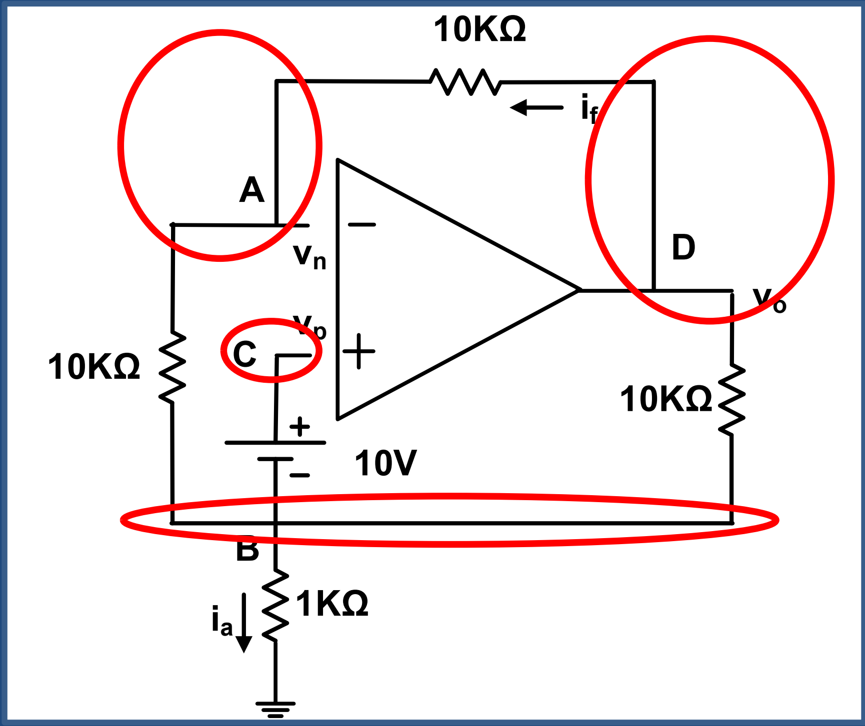
$v_C - v_B = 10$

But $v_C = v_A = v_P = v_n \Rightarrow v_A - v_B = 10$ (3)

(1) & (2) => $3v_A - 13v_B = 0$ (4)

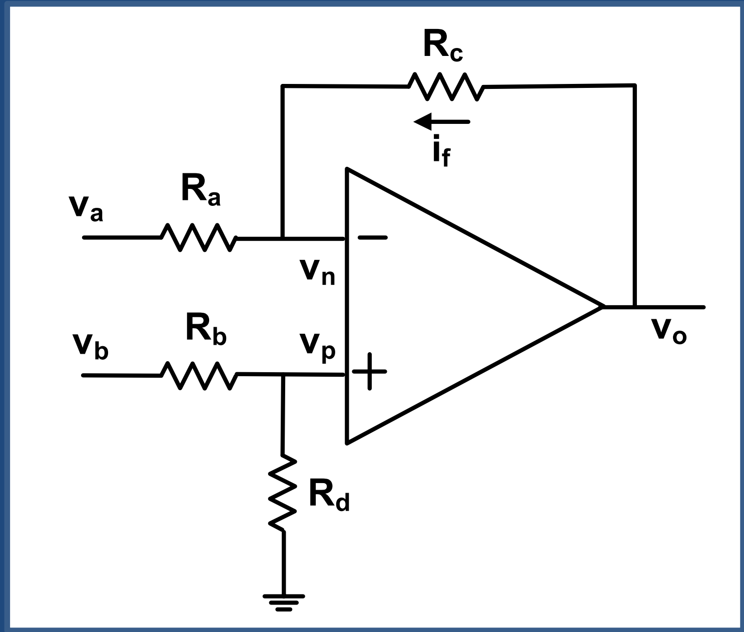
(3) & (4) => $v_B = 3V$

=> $i_a = \frac{3}{1K}$ = **3mA**



Difference Amplifier

1. The goal of this circuit is to:
   - Compare 2 inputs
   - Eliminate the noise
   - Amplify the difference between 2 inputs
2. $i_p = i_n = 0$
3. $v_p = v_n$



Difference Amplifier

Use node technique:

A: $(\frac{1}{R_a} + \frac{1}{R_c})v_n - \frac{1}{R_a}v_a - \frac{1}{R_c}v_o = 0$ (1)

B: $(\frac{1}{R_b} + \frac{1}{R_d})v_p - \frac{1}{R_b}v_b = 0$ (2)

(1) => $v_o = (\frac{R_c}{R_a} + 1)v_n - \frac{R_c}{R_a}v_a$ (1')

(2) => $v_p = \frac{R_d}{R_b+R_d} v_b = v_n$ (2')

$\Rightarrow v_o = (\frac{R_a + R_c}{R_a})(\frac{R_d}{R_b+Rd})v_b - \frac{R_c}{R_a}v_a$ (3)

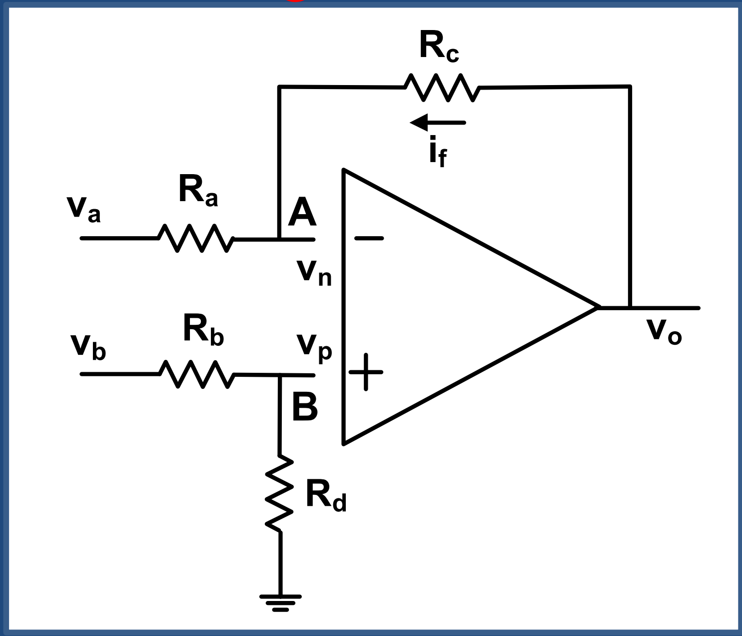
To eliminate the noise i.e., $v_o = 0$ when $v_a = v_b$

(3) => $(\frac{R_a + R_c}{R_a})(\frac{R_d}{R_b+Rd}) = \frac{R_c}{R_a}$

Or $R_aR_d = R_bR_c$

and $v_o = \frac{R_c}{R_a}(v_b - v_a)$

Gain



Difference Amplifier: Exercise

Design this circuit with gain = 10X, R_a = 4.7KΩ and voltage source v_b sees an input resistance of 220KΩ.

Gain = 10

$R_a R_d = R_b R_c$ (1)

$v_o = \frac{R_c}{R_a}(v_b - v_a)$ (2)

(1) => $4.7K \times R_d = R_b R_c$

$\frac{R_c}{4.7K} = 10$ => $\mathbf{R_c = 47K\Omega}$

and (1) => $\frac{R_d}{R_b} = \frac{R_c}{R_a} = 10$

=> $R_d = 10\ R_b$ (3)

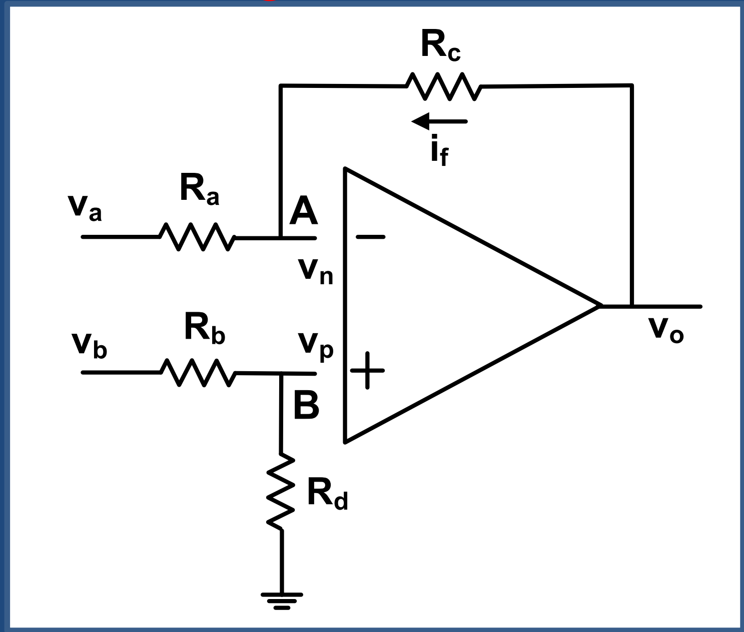
V_b sees an output resistance of 220K

i.e., $R_b + R_d = 220K\Omega$ (4)

(3) & (4) => $R_b + 10R_b = 220K\Omega$

$\Rightarrow$ $\mathbf{R_b = 20K\Omega}$

and $\mathbf{R_d = 200K\Omega}$



Difference amplifier: Another perspective

- Differential mode input

$V_{dm} = v_b - v_a$

- Common mode input

$V_{cm} = (v_a + v_b)/ 2$

- $V_a = v_{cm} - (1/2)\, v_{dm}$
- $V_b = v_{cm} + (1/2)\, v_{dm}$
- $V_0 = A_{cm}\, v_{cm} + A_{dm}\, v_{dm}$
  - ❖ A_{cm} : common mode gain

$$A_{cm} = \frac{R_d(R_a+R_c)}{R_a(R_b+R_d)} - \frac{R_c}{R_a}$$

  - ❖ A_{dm} : differential mode gain

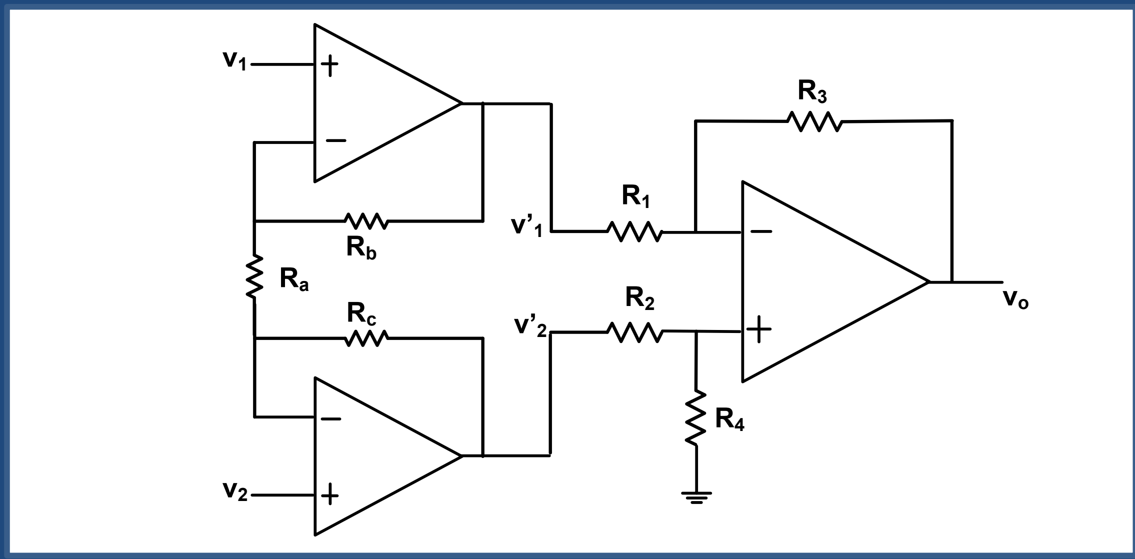
$$A_{dm} = \frac{1}{2}\left[\frac{R_d\,(R_a+R_c)}{R_a(R_b+R_d)} + \frac{R_c}{R_a}\right]$$

- Common mode rejection ratio:

CMRR $= |A_{dm}/A_{cm}|$ (the higher the better)

Instrumentation amplifier

1. Ultrahigh input impedance: 10^{15} ohm
2. High and stable linear gain: 10 to 1,000
3. High Common Mode Rejection Ratio (CMRR): >10,000 or 60-100 dB



Precision Instrumentation Amplifier

AD524

FEATURES

Low noise: 0.3 μV p-p at 0.1 Hz to 10 Hz
Low nonlinearity: 0.003% (G = 1)
High CMRR: 120 dB (G = 1000)
Low offset voltage: 50 μV
Low offset voltage drift: 0.5 μV/°C
Gain bandwidth product: 25 MHz
Pin programmable gains of 1, 10, 100, 1000
Input protection, power-on/power-off
No external components required
Internally compensated
MIL-STD-883B and chips available
16-lead ceramic DIP and SOIC packages and 20-terminal leadless chip carrier available
Available in tape and reel in accordance with EIA-481A standard
Standard military drawing also available

FUNCTIONAL BLOCK DIAGRAM

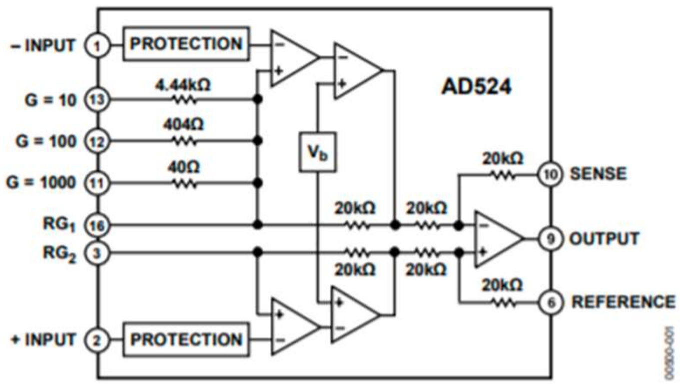


Figure 1.

GENERAL DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common-mode rejection, low offset voltage drift, and low noise makes the AD524 suitable

higher linearity C grade are specified from −25°C to +85°C. The S grade guarantees performance to specification over the extended temperature range −55°C to +125°C. The AD524 is available in a 16-lead ceramic DIP, 16-lead SBDIP, 16-lead SOIC wide packages, and 20-terminal leadless chip carrier.

Võ Văn Tới
School of Biomedical Engineering
International University of Vietnam National Universities
HCM City, Vietnam
Email: vvtoi@hcmiu.edu.vn
Website: www.hcmiu.edu.vn/bme